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On the Delay of a CNTFET with Undeposited CNTs by Gate Width Adjustment

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Abstract This paper deals with the performance of a Carbon Nano Tube Field Effect Transistor (CNTFET) in the presence of undeposited CNTs as defects. A simulation-based analysis of delay degradation due to different features (such as chirality and defective CNT distribution) is initially pursued. Two solutions to mitigate the change in delay are proposed; these approaches are based on adjusting the gate width of the CNTFET by lithography (and removing CNTs) as part of the fabrication process. These two methods reduce the average delay and its deviation, respectively. A probabilistic delay analysis is then presented. The performance of the proposed two adjustment methods is evaluated by considering CNT features (such as chirality and defect distribution) deterministically and probabilistically. By deterministic (probabilistic) simulation, the first method reduces on average the delay by 6.968 % (7.811 %) while the deviation is increased (decreased) by 32.444 % (9.788 %). The second method reduces deterministically (probabilistically) on average the deviation by 44.159 % (47.476 %) with 2.166 % (4.409 %) delay reduction.

Keywords Defect modeling · CNT · CNTFET · Manufacturing · Emerging technologies

1 Introduction

The Carbon NanoTube Field Effect Transistor (CNTFET) is one of the most promising emerging technologies to extend and complement the silicon MOSFET; this is due to its excellent performance characteristics and similarity in operational principles and device structure [6, 7]. During manufacturing, CNTs are usually grown or transferred to a substrate with a fixed pitch prior to defining the gates and the contacts. Some of the likely defects that may occur when manufacturing CNTFETs are the absence of deposited CNTs. These defects significantly affect the performance of the CNTFET, because the current flowing in each CNT is changed. Moreover, as the number of CNTs present in the channel is reduced and the distances between them are uneven, changes of current and gate capacitance are encountered [3, 6, 7, 16].

For estimating the performance of a CNTFET, various simulation models have been proposed [3, 4, 8, 15]. The HSPICE model of [4, 6, 7] is widely used in CNTFET circuit design. However, only the scenario of constant pitch between CNTs in a CNTFET is considered, i.e. the effect of uneven spacing caused by undeposited CNTs cannot be taken into consideration. A MATLAB-based model for a CNTFET with undeposited CNTs has been proposed [3]. Using this model, a CNTFET can be estimated with respect to the effects of undeposited CNTs; it has been shown that the performance of a CNTFET can be affected by the number and position of the undeposited CNTs. The delay in a CNTFET significantly increases with the number of undeposited CNTs and the deviation in delay depends on the position of the undeposited CNTs. While the model of [3] offers significant advantages in terms of electrical characteristics (such as current and gate capacitance), the the analysis of a CNTFET in the presence of undeposited CNTs remains elusive and its overall performance is still unpredictable in the presence of these defects.

This paper initially considers both the number and position of the undeposited CNTs to estimate the delay degradation and its deviation. This detailed analysis shows that when the undeposited CNTs are grouped together (the deposited

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CNTs are separated by the least intervals), the delay has a small value. When the deposited CNTs are separated by the largest intervals, then the delay becomes the largest. Subsequently, a probabilistic analysis is presented to estimate the impact of undeposited (defective) CNTs on the delay of a CNTFET. In general, when the intervals decrease, the drain current decreases due to the screening effect; the gate capacitance also decreases due to the decrease of the gate-to-channel capacitance. The effect of chirality is also estimated with respect to the delay. Simulation results show that these features (the diameter, the number and position of the CNTs) severely affect the operation of a CNTFET. Therefore, a corrective method is required to increase the performance of a CNTFET and to reduce the effect of undeposited CNTs. In today's technology, corrective processes must be employed when manufacturing CNTFETs; for example, defective CNTs (such as misaligned CNTs) can be removed by using electrical breakdown and selective etching [5, 9]. Techniques for detection and correction have been also proposed [10]. So, a new corrective action for the fabrication process is suggested in this paper; based on the capabilities of today's lithography, two methods are proposed. The first method reduces the delay, while the second method reduces its deviation. These methods decrease the gate capacitance of the CNTFET by adjusting the gate width of the CNTFET; extensive simulation results are performed deterministically and probabilistically to show the application of these methods to CNTFETs of different chirality and undeposited CNTs.

2 Review of CNTFET

The structure of a CNTFET is illustrated in Fig. 1 [6, 7]; a CNTFET is usually manufactured by depositing CNTs (as sheets of graphene rolled into tubes) to a substrate. This effectively defines the channel between drain and source; the CNTs have fixed spacing (pitch) prior to defining the gates and the contacts. The chirality (i.e., the angle/direction in which the graphene sheet is rolled) of the CNT determines its diameter. A CNT can be also either metallic or semiconducting depending on the chirality. In this paper, only single-walled semiconducting CNTs are analyzed.

The common steps for manufacturing a CNTFET are shown in Fig. 2 [5, 9, 10]. Figure 2a shows that CNTs are deposited to a substrate. Then, the region of logic cells is defined using lithography and the CNTs outside this region are etched away (Fig. 2b). One of the likely defects that occur during the deposition of the CNTs is that only some of the required CNTs are deposited. In this paper, it is assumed that in the presence of undeposited CNTs (as identified by empty spacing), the remaining (deposited) CNTs are semiconducting and aligned. Figure 2 (c) shows the gate and contact regions as defined by lithography in the presence of undeposited CNTs. The last manufacturing step (Fig. 2d) is then implemented and the CNT regions corresponding to the PFET (NFET) transistors are doped accordingly.

To evaluate the performance of a CNTFET, various simulation models have been proposed [3, 4, 8, 15]. The HSPICE model of [4] is widely used in CNTFET circuit design. However, even spacing between CNTs is assumed in [4, 6, 7]; so, the effect of uneven spacing due to undeposited CNTs in a CNTFET cannot be evaluated. [3] has proposed a MATLAB-based model for a CNTFET with undeposited CNT defects. As shown in Fig. 3 [3], the positions of the deposited CNTs are given by the Boolean vector P_{CD} also referred to as *configuration*. The configuration denotes the state of the CNTFET with respect to the CNT defects. In P_{CD}, the ith bit of the binary string is 0 (1) if the ith CNT is undeposited (deposited). Figure 3 shows a $P_{CD}=\{1\ 0\ 1\ 1\ 0\ 1\ 0\ 0\ 1\}$ when the number of undeposited CNTs (denoted by N_{CD}) is 4. In the presence of undeposited CNTs, the deposited CNTs are separated by uneven spacings as function of the pitch (s) (s=3.812 nm when the gate width (W_g) is 32 nm and the total number of CNTs in a CNTFET (N) is 9 for a (19,0) chirality); therefore, deposited CNTs are aligned with different intervals (denoted as 'int_a', 'int_b', 'int_c', and 'int_d') and each *int* in a CNTFET is a multiple of the pitch (i.e. s). For example, $int_a=2s$, $int_b=1s$, $int_c=2s$, and $int_c=3s$. [3] has reported that a performance degradation occurs in a CNTFET; this is related to N_{CD} and P_{CD} (Fig. 4). The delay rapidly increases with N_{CD} because the CNTs are used as channel between the drain and source of a CNTFET. The change in the delay is mostly caused by P_{CD} (at a fixed N_{CD}), but it depends also on N_{CD}.

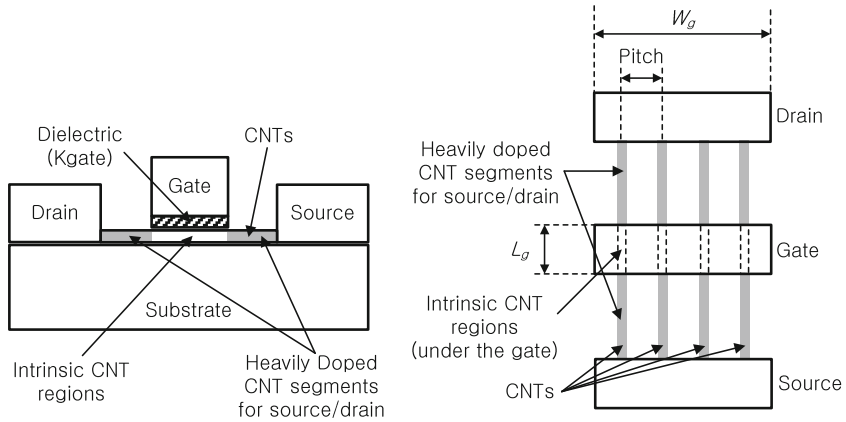
3 Delay Analysis by N_{CD} and P_{CD}

Depending on N_{CD} and P_{CD}, the undeposited CNTs may have different positions in a CNTFET. So, all possible (combinatorial) values of N_{CD} and P_{CD} must be considered when analyzing the performance of a CNTFET [3]. Let the number of combinations for the undeposited CNTs be denoted by N_{CCD}, i.e.

$$N_{CCD} = \binom{N}{N_{CD}} = \frac{N!}{N_{CD}! \times (N-N_{CD})!} \tag{1}$$

An algorithm for the Deterministic Analysis (DA) of the delay of a CNTFET with undeposited CNTs is proposed in this section using the model of [3] for the capacitance and current. This algorithm (referred to as Algorithm 1) utilizes a

Fig. 1 CNTFET structure

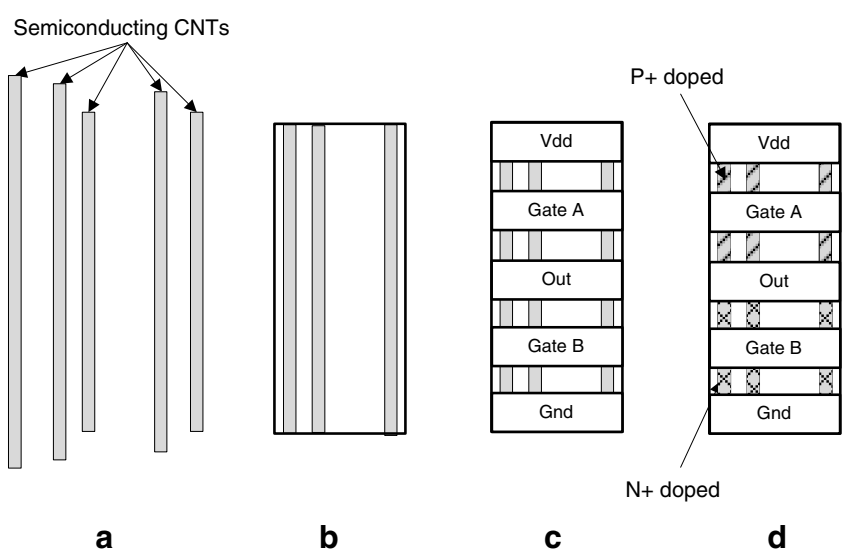


combinatorial routine (i.e. nchoosek in MATLAB) for finding all possible P_{CD}'s combinations (denoted by N_{CCD}); every *i*th combination in the CNTFET is considered. Within each P_{CD}, both intervals for the deposited CNTs are established; for every *j*th CNT, both of its intervals are denoted as $int_1(j)$ and $int_2(j)$. Based on the values of the intervals, the gate-to-channel capacitance (C_{gc}) is determined [3]. Subsequently, the gate capacitance of the CNTFET and the current of each CNT are calculated [3] (where the current of the CNTFET can be found by adding the currents of all of its CNTs). The delay in CNTFET operation is calculated using the widely used delay equation *CV/I* [6, 7, 14]. The *Relative Standard Deviation (RSD)* is used to estimate the deviation (as the difference between the largest value ($V_{LARGEST}$) and least value (V_{LEAST})) from the average value (V_{AVG}) of the drain current, gate capacitance and delay). RSD is given in (2) and plotted in Fig. 5; the RSDs for the rates of change in drain current and capacitance have different percentage values.

$$RSD = \sqrt{(V_{LARGEST} - V_{AVG})^2 + (V_{AVG} - V_{LEAST})^2} \times \frac{100}{V_{AVG}} \quad (2)$$

Both drain current and gate capacitance vary as function of C_{gc} (related to the intervals int_1 and int_2 of each CNT). However, the rate of change for the gate capacitance is larger than for the drain current; so, the RSD for the delay is mostly affected by the gate capacitance (Fig. 5). Moreover, the configuration at which the deviation of the gate capacitance has the largest value is not the same as for the current. This occurs because the gate capacitance ($C_{gg,CNTFET}$) is affected not only by the gate-to-channel capacitance (C_{gc}) but also by the gate-to-gate capacitance (C_{gtg}) and the gate width (W_g) [3]. (1) is also plotted in Fig. 5 at a chirality vector of (19,0). N_{CCD} has maximum value when N_{CD} is 4 and 5; however the largest deviation for the delay does not occur at the largest value of N_{CCD}. So, a more detailed analysis involving P_{CD} is required.

Fig. 2 CNTFET manufacturing process



```
Algorithm Delay
begin
   do by choosing N_CD from N
   for i to N_CCD
      for j to N-N_CD
         if int1(j)=0 or int2(j)=0
            C_gc_p(j)=C_gc_e (int1(j), int2(j))
         else if int1(j)==int2(j)
            C_gc_p(j)=C_gc_m_symmetric(int1(j))
         else
            C_gc_p(j)=C_gc_m_assymetric(int1(j), int2(j))
         end
         C_gc(i) ⋃ {C_gc_p(j)}
         Total_I(i) ⋃ I_semi(V_GS, V_DS, C_gc_p(j))
      end
      C_gg,CNTFET(i)(W_g, L_g, C_gc(i))
      Delay_gg,CNTFET(i)=( 4·C_gg,CNTFET(i)·V)/ Total_I(i)
   end
end
```

Algorithm 1. Delay in a CNTFET with Undeposited CNTs [3]

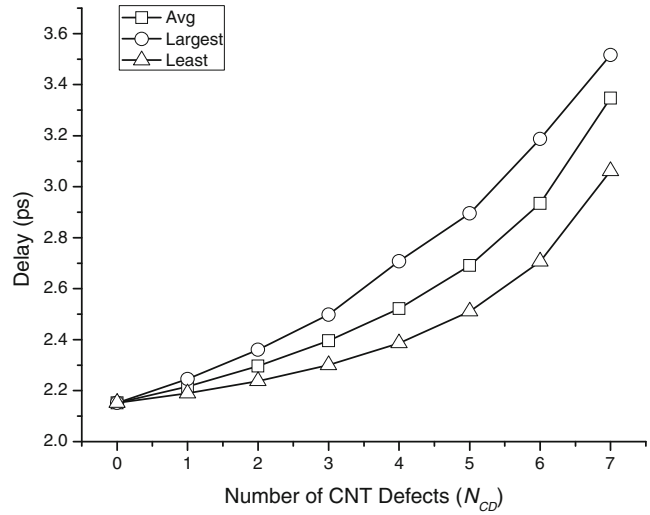


Fig. 4 Delay vs. N_{CD} (V_{GS}=0.9 V, (19,0), N=9, W_g=32 nm) [3]

Depending on P_{CD}, the variations in current, capacitance and delay (at a fixed N_{CD}) occur due to the intervals caused by the presence of undeposited CNTs. Figures 6 and 7 show the sum of two intervals between CNTs (int_1+int_2) for the largest and least delays respectively; for example, when N_{CD}=6 (chosen because the RSD of the delay has the highest value as plotted previously in Fig. 5), there are three deposited CNTs in the CNTFET (Fig. 8). The P_{CD} for the largest delay is shown in Fig. 8a; the two-CNT intervals are 0 and 4s (nm) (int_1=0 and int_2=4s) where'0'means there is no adjacent CNT (i.e. there is no significant distance, that can change the gate capacitance and current of the CNTFET between the CNTs) as the CNT is positioned at the edge and the one-CNT intervals are 4s and 4s

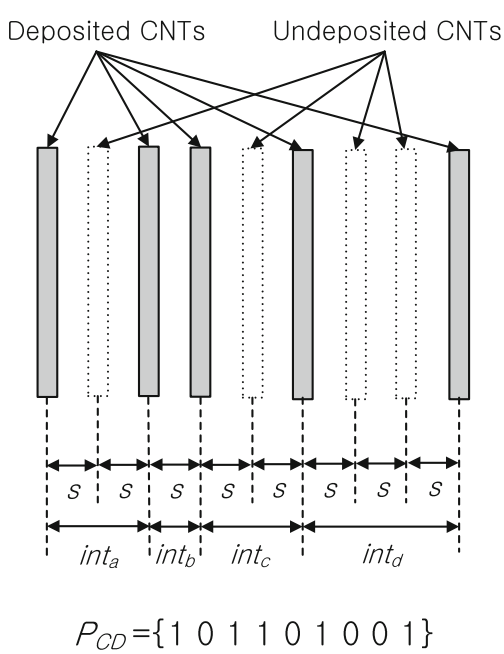


Fig. 3 CNTFET with undeposited CNTs and intervals [3]

(int_1=4s and int_2=4s). So, the sum of the two-CNT intervals is 4s (int_1+int_2=4s) and the sum of the one-CNT intervals is 8s (int_1+int_2=8s). In Fig. 8b, c, and d (for the P_{CD} of least delay), the sum of the two-CNT intervals is 1s (int_1+int_2=1s) and the sum of one-CNT intervals is 2s (int_1+int_2=2s).

As reported in Figs. 6, 7 and 8, when the deposited CNTs are separated by the largest interval, then the delay is the largest. The delay has the least value when the deposited CNTs are grouped together (i.e. with the least intervals). So, when the intervals decrease, the drain current decreases due to the screening effect; the gate capacitance also decreases due to a decrease of C_{gc} [6, 7]. Figures 6 and 7 show that the delay decreases because it is mostly affected by the gate capacitance (in the *CV/I* equation); moreover, these results are consistent with the results for the RSDs in Fig. 5.

4 Probabilistic Delay Analysis

In this section, a Probabilistic Analysis (PA) is pursued for a given P_{CD} based on [3]. Let the probability of occurrence for a P_{CD} be denoted by $PROB_{PCD}$,; moreover, let the *random variable* for the number of undeposited CNTs be denoted as X_{CD} with range S= {0,1,…,N}. X_{CD} is assumed to be *independently distributed* and the probability of undeposited CNTs is denoted by p_{CD} (0≤p_{CD}≤1). Then, $PROB_{PCD}$ can be written as below using the well known Bernoulli probability expression.

$$PROB_{PCD}[X_{CD} = N_{CD}] = \binom{N}{N_{CD}} \times P_{CD}{}^{N_{CD}} \times (1-P_{CD})^{(N-N_{CD})} \times 100 \quad (3)$$

Using Eq. 1, Eq. 3 can be written as

$$PROB_{PCD}[X_{CD} = N_{CD}] = N_{CD} \times P_{CD}{}^{N_{CD}} \times (1-P_{CD})^{(N-N_{CD})} \times 100 \quad (4)$$

For current technology, CNT synthesis techniques yield at most 33 % metallic CNTs, for example, [13] has reported 4 %

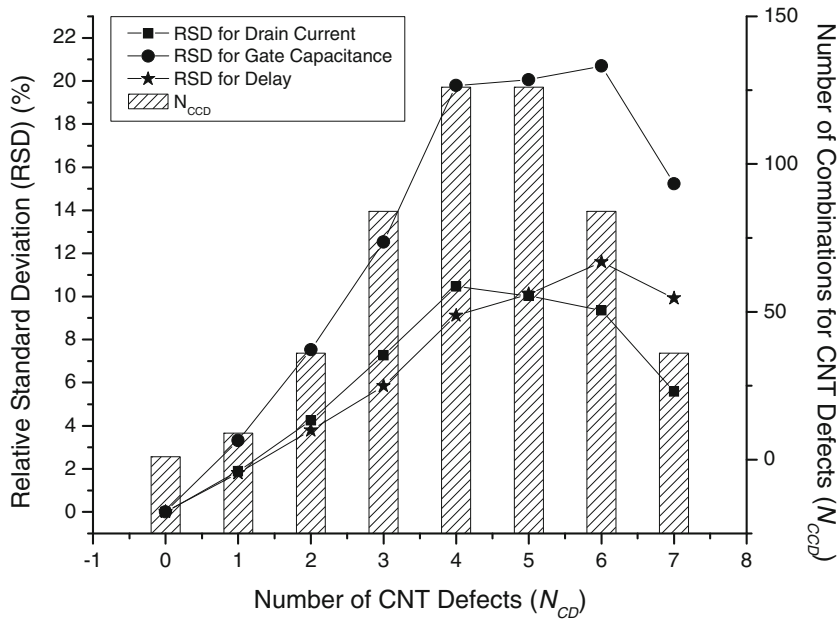


Fig. 5 RSD and N_{CCD} vs. N_{CD} (V_{GS}=0.9 V, (19,0), N=9, W_g=32 nm) [3]

metallic CNTs. Other CNT defects (due to erroneous positioning and alignment) can occur [12]; 99.5 % of all CNTs can be correctly aligned when the average density of the CNTs is 5–10 CNTs/μm. However, 250 CNTs/μm are required to ensure a performance (delay and energy) better than CMOS [11]; so, this higher CNT density is used in this paper to measure the performance degradation. Compared with [12], at least a 10 % decrease in probability of correct alignment can be expected for more than two orders of magnitude increase in density [2], i.e. it is assumed that 90 % of all CNTs are aligned when the CNT density is 250 CNTs/μm. As no exact relation has been yet established between the presence of metallic CNTs and mispostioned (and misaliged) CNTs, p_{CD} is calculated probabilistically as given below [1]

$$\begin{aligned} p_{CD} &= p_{CD_Metallic} + p_{CD_Mis-positioned} - p_{CD_Metallic} \times P_{CD_Mis-positioned} \\ &= 0.04 + 0.2 - 0.04 \times 0.2 \\ &= 0.232 \end{aligned} \tag{5}$$

$PROB_{PCD}$ is calculated as a function of N_{CD} using Eq. 4; the results are plotted in Fig. 9. The increases in average delay (in % in Fig. 4) and RSD (in % in Fig. 5) are also depicted in Fig. 9. $PROB_{PCD}$ increases when N_{CD} is 1 and 2, but $PROB_{PCD}$ decreases as N_{CD} increases to higher values. Moreover, a degradation occurs for the average delay and RSD when N_{CD} has a small value; the average delay increases significantly as N_{CD} increases. Let the number of configurations with the same interval(s) be denoted as N_{PCD}; N_{PCD} is dependent on the interval values, N_{CD} and N, i.e. the values of $PROB_{PCD}$ that result in the largest ($PROB_{PCD_Largest}$) or least delay ($PROB_{PCD_Least}$), depend on N_{CD} and N. They are calculated using Eq. 4, as

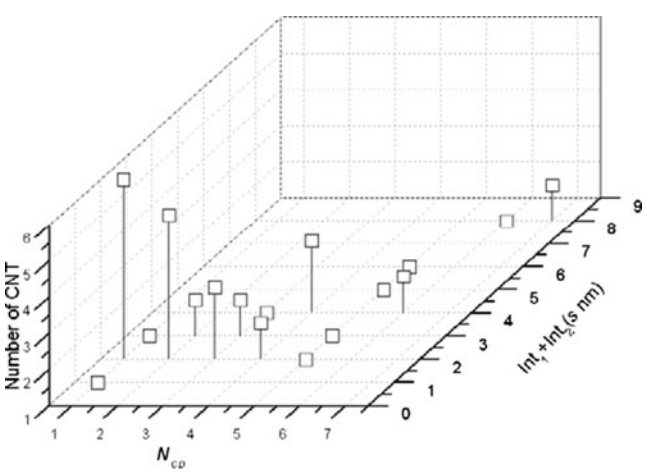


Fig. 6 Sum of two intervals between CNTs (int_1+int_2) for largest delay vs. N_{CD} (V_{GS}=0.9 V, (19,0), N=9) [3]

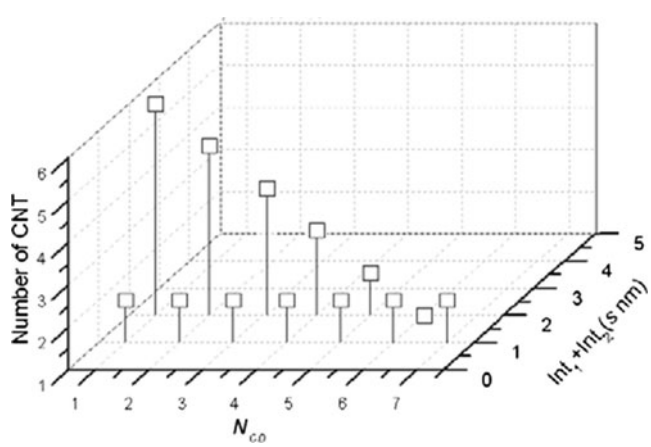


Fig. 7 Sum of two intervals between CNTs (int_1+int_2) for least delay vs. N_{CD} (V_{GS}=0.9 V, (19,0), N=9) [3]

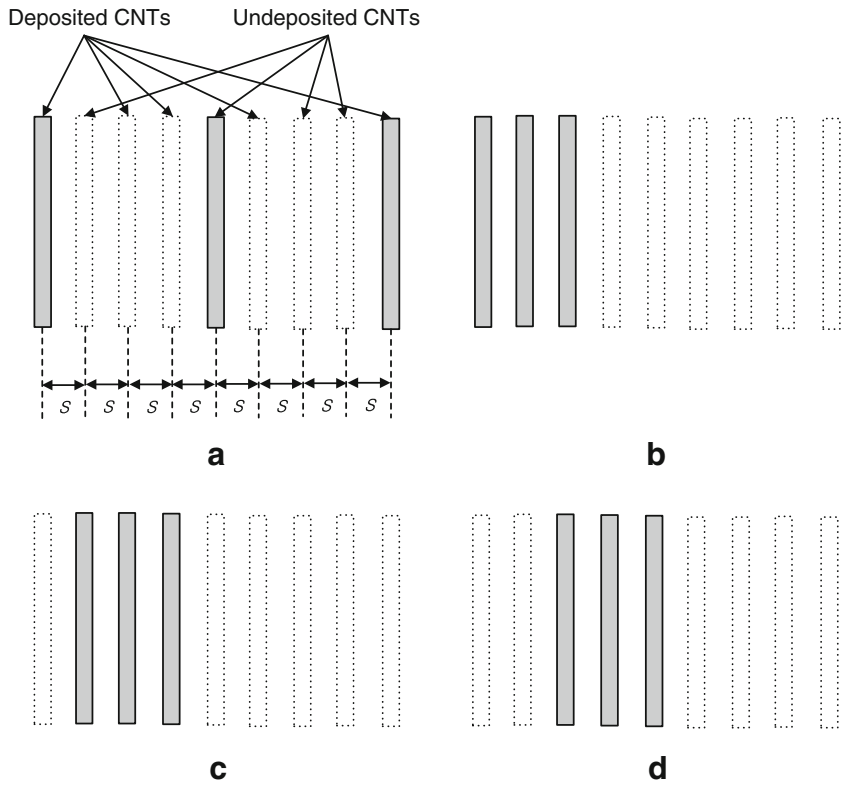


Fig. 8 P_{CD} for largest delay (**a**) and P_{CD} for least delay (**b**, **c**, and **d**) (V_{GS}=0.9 V, (19,0), N=9, N_{CD}=6, W_g=32 nm) [3]

$$PROB_{PCD_Largest} = \left(N_{PCD_Largest} \big/ N_{CCD}\right) \times PROB_{PCD}$$
$$PROB_{PCD_Least} = \left(N_{PCD_Least} \big/ N_{CCD}\right) \times PROB_{PCD} \quad (6)$$

$N_{PCD_Largest}$ and N_{PCD_Least} can be found by selecting the configurations with the largest and least delays for $C_{gg,CNTFET}$ in Algorithm 1 (with N_{CD} and N as inputs). $PROB_{PCD_Largest}$, $PROB_{PCD_Least}$, $N_{PCD_Largest}$, N_{PCD_Least}, and N_{CCD} are reported for N=9 as function of N_{CD} in Table 1. $PROB_{PCD_Largest}$ is less than $PROB_{PCD_Least}$ because, in general, $P_{CD_Largest}$ requires configurations with large intervals and the number of these configurations is small. Similarly, P_{CD_Least} is found in configurations with small intervals; so, many configurations exist (Fig. 8b, c, and d) and N_{PCD_Least} increases linearly with N_{CD} (Table 1). This plot shows a different characteristic; when N_{CD} is 4 and 5, N_{CCD} has the largest value. However, N_{CCD} decreases when N_{CD} is not between 4 and 5. $PROB_{PCD_Largest}$ and $PROB_{PCD_Least}$ are affected more by N_{CCD} than N_{PCD_Least} because N_{CCD} has a value larger than N_{PCD}.

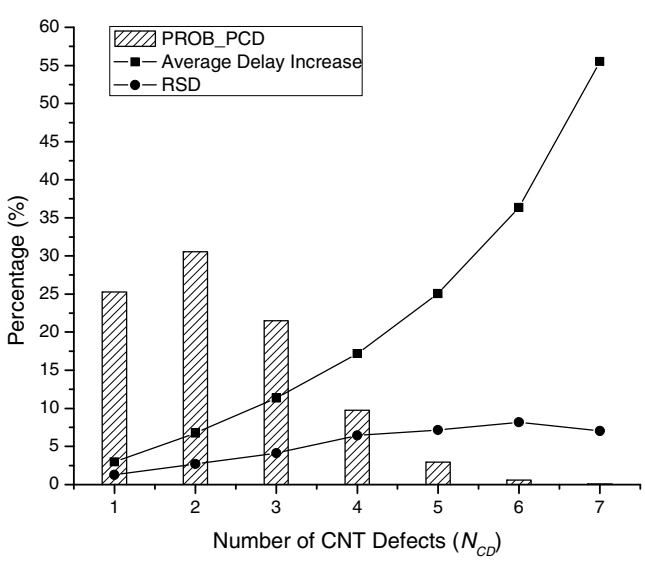


Fig. 9 $PROB_{PCD}$, delay increase, and RSD vs. N_{CD} (V_{GS}=0.9 V, (19,0), N=9, W_g=32 nm) [3]

In Fig. 9 and Table 1, $PROB_{PCD}$ is calculated by assuming that p_{CD} is fixed to 0.232 (as found in Eq. 5). However, this is dependent on the manufacturing technology. In the probabilistic analysis for p_{CD}, it is assumed that p_{CD} is normally distributed. When N_{CD} is determined from the distribution, only integer values between from 0 to 7 (for the (19,0) chirality) are used. After N_{CD} is determined, P_{CD} is randomly selected based on a uniform distribution. Figure 10 shows the delay for different mean and standard deviation (σ) values under a normal distribution. When the mean value is changed from 0 to 0.9 (Fig. 10a), the average delay values remain almost unchanged even at different standard deviation values; however, as shown in Fig. 10-b, when the standard deviation increases, the largest (least) delay value increases (decreases). Moreover both these delay values saturate because a value higher (smaller) than 7 (0) cannot be used for N_{CD} when the standard deviation increases.

Table 1 Probability of P_{CD} for largest delay and least delay (V_{GS}=0.9 V, (19,0), N=9) [3]

Probability	N_{CD}						
	1	2	3	4	5	6	7
$PROB_{PCD_Largest}$ (%) ($N_{PCD_Largest}$, N_{CCD})	5.616 (2,9)	0.848 (1,36)	0.513 (2,84)	0.077 (1,126)	0.047 (2,126)	0.007 (1,84)	0.002 (1,36)
$PROB_{PCD_Least}$ (%) (N_{PCD_Least}, N_{CCD})	5.616 (2,9)	2.545 (3,36)	1.025 (4,84)	0.387 (5,126)	0.140 (6,126)	0.049 (7,84)	0.017 (8,36)

5 Delay and Chirality

The CNT diameter is a significant parameter for CNTFET design [11]. As P_{CD} and N_{CD} affect the current and the capacitance of a CNTFET, so a change of CNT diameter (resulting from the chirality) also causes a change of current, gate capacitance and threshed voltage in a CNTFET [6, 7]. Therefore, when P_{CD} and N_{CD} are considered for delay analysis, the effects of a change in CNT diameter must also be estimated. In a CNTFET, the diameter is determined by the chirality vector, (n, m). Only 'n' is changed in this paper for those values of semiconducting CNTs only.

Figure 11 shows the effect of the diameter when N_{CD} is changed. At a fixed chirality, the trends for the change in average, largest, and least values are similar to Fig. 4, but these trends are also function of the chirality. When the chirality changes, the delay does not change linearly, i.e. the current and the gate capacitance do not have a linear relationship with the chirality [6, 7]. Consider the change in the diameter for the simulation results of Fig. 10 (in which p_{CD} is normally distributed); Figures 12 and 13 show similar plots to Fig. 10 (Fig. 12 shows only the average values, while Fig. 13 shows the largest and least values).

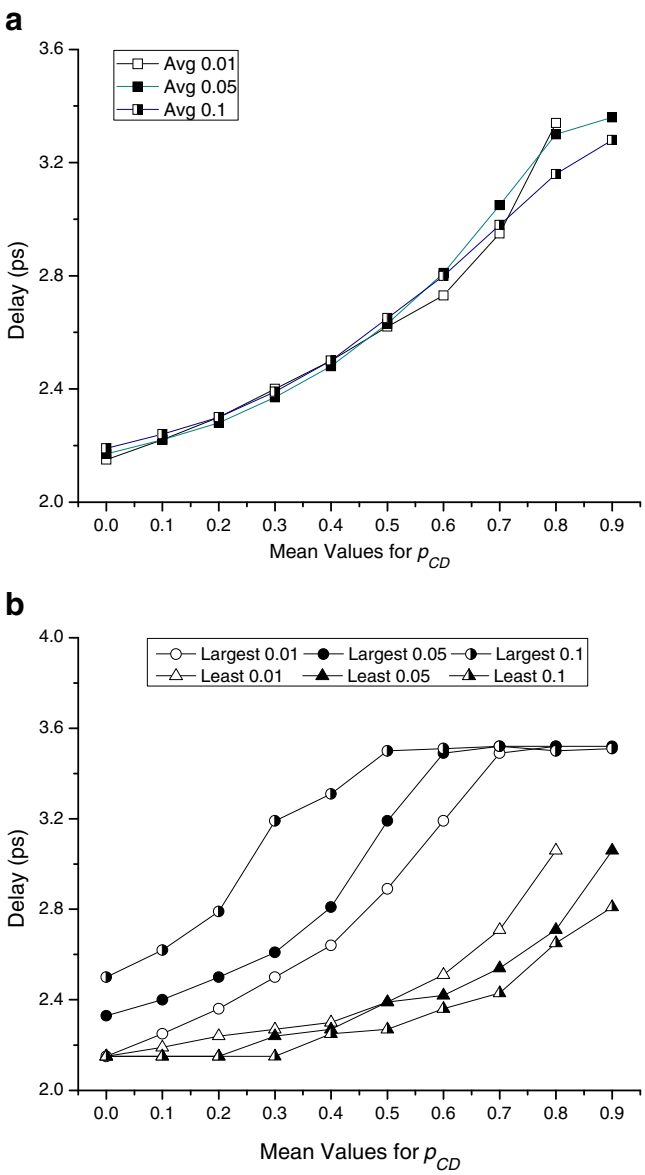


Fig. 10 Delay (**a** average value and **b** largest (least) values) vs. mean values for the probability of p_{CD} at various standard deviations under a normal distribution (V_{GS}=0.9 V, (19,0), N=9, W_g=32 nm)

6 Gate Width Adjustment

As shown previously, the delay in a CNTFET significantly changes as function of P_{CD}, N_{CD} and chirality. Consider the fabrication process of a CNTFET. When the regions of logic

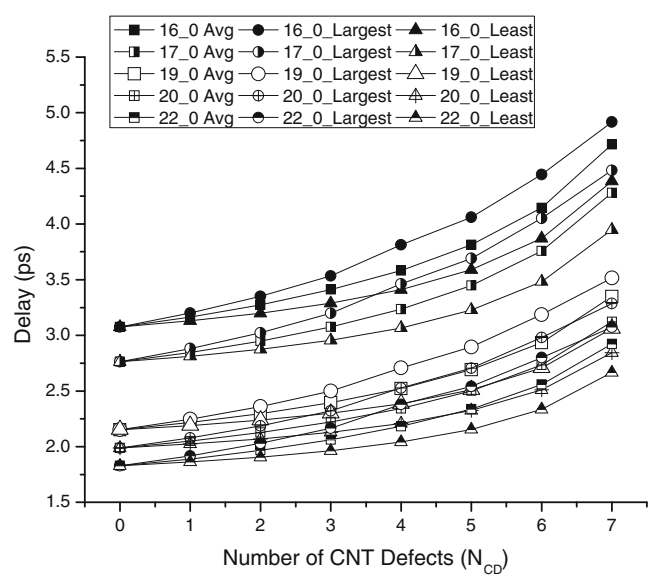


Fig. 11 Delay at different chirality vs. N_{CD} (V_{GS}=0.9 V, N=9, W_g=32 nm)

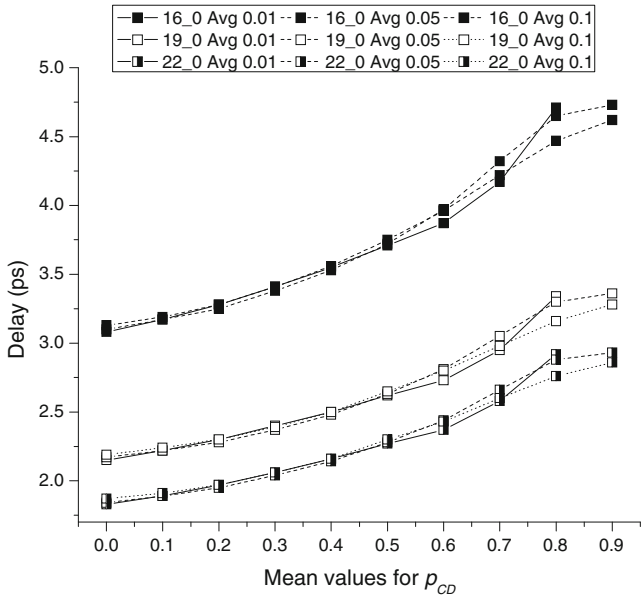


Fig. 12 Average delay values vs. mean values for p_{CD} at various values of standard deviation and chirality (V_{GS}=0.9 V, N=9, W_g=32 nm)

cells and contacts are defined (as shown in Fig. 2b and c respectively), predefined layouts are usually used. However, current imaging and process technologies [16] make possible to estimate N_{CD}, P_{CD}, and the intervals prior to defining the logic cells and the contacts. In [16], the CNT spacing distribution is extracted using a Scanning Electron Microscope (SEM); moreover, a partial etching step is possible for the adjustment of this area [5, 9, 10]. Therefore, the process of gate width adjustment can be performed by considering N_{CD} and P_{CD} and using current fabrication/manufacturing technology.

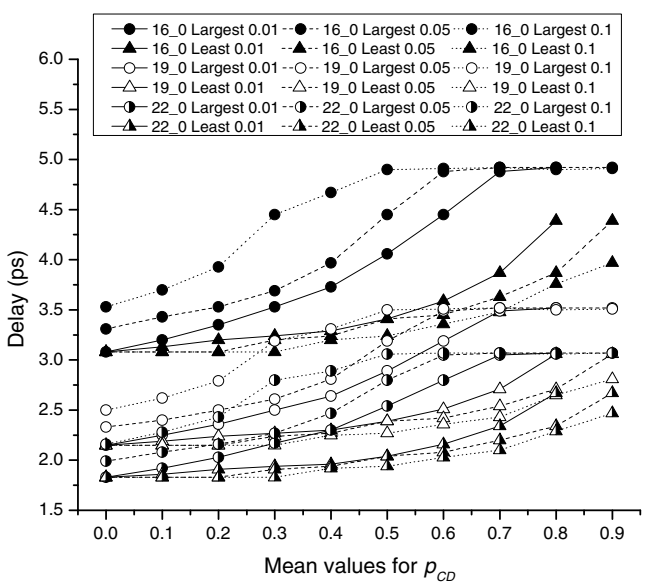


Fig. 13 Largest and least delay values vs. mean values for the probability of p_{CD} with various standard deviation and chirality (V_{GS}=0.9 V, (19,0), N=9, W_g=32 nm)

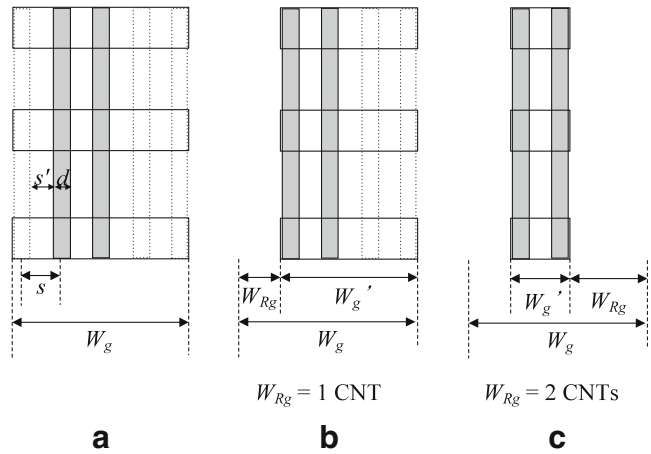


Fig. 14 Reducing W_g (W_{Rg}=1 CNT and W_{Rg}=2 CNTs)

When the gate and contact regions are defined (Fig. 2c), the drain current and gate capacitance of a CNTFET can be decreased by reducing the gate width as shown in Fig. 14. However, the changes in drain current and gate capacitance depend on N_{CD}, P_{CD} and chirality. Therefore, the process of adjusting the gate width is utilized by considering those parameters (N_{CD},

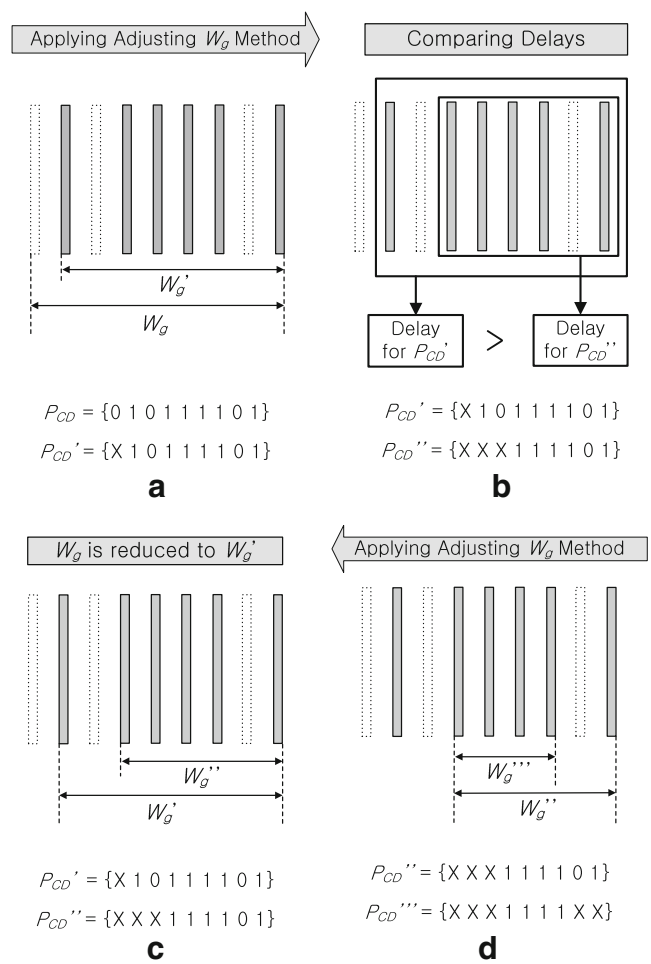


Fig. 15 Proposed method for W_g adjustment

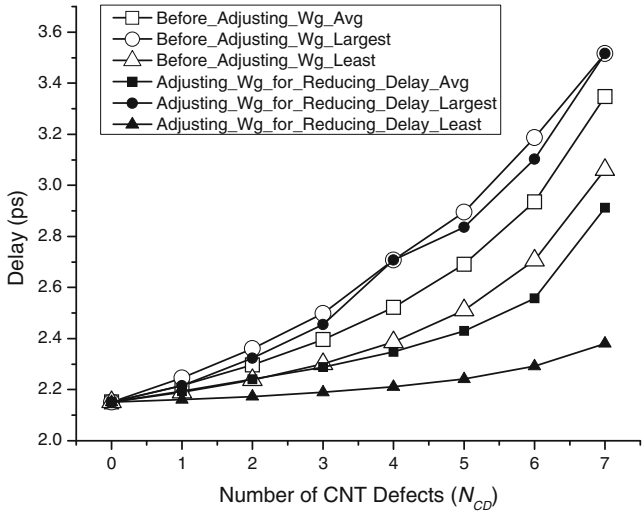


Fig. 16 Delay vs. N_{CD} with adjusting W_g for reducing delay (Algorithm 2) (V_{GS}=0.9 V, (19,0), N=9, W_g=32 nm)

P_{CD} and chirality). Two methods (one is for reducing the delay and the other for reducing the deviation) are proposed in this paper based on this approach. To adjust the gate width, the reduction of W_g is measured in units of CNTs (W_{Rg} in Fig. 14); Figure 14a shows that a CNTFET contains two deposited CNTs (solid lines) and three undeposited CNTs (dotted lines). So, W_{Rg}=1 CNT and W_{Rg}=2 CNTs in Fig. 14b and c respectively. Figure 14a shows the pitch (s), the distance between two CNTs (s'), and the diameter of the CNT (d) in the CNTFET. The relationship among these parameters in Fig. 14 is given in Eq. 7. Equation 7 shows that the reduction in W_g with units of number of CNTs is the same as reducing W_g with the unit of 's', i.e. W_{Rg}=1 CNT and W_{Rg}=2 CNTs in Fig. 14 are equivalent and consistent with $W_{Rg}=1s$nm and $W_{Rg}=2s$nm.

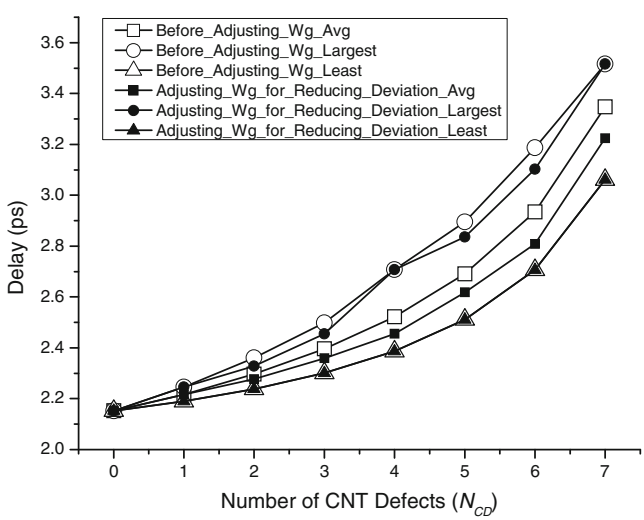


Fig. 17 Delay vs. N_{CD} with adjusting W_g for reducing deviation (Algorithm 3) (V_{GS}=0.9 V, (19,0), N=9, W_g=32 nm)

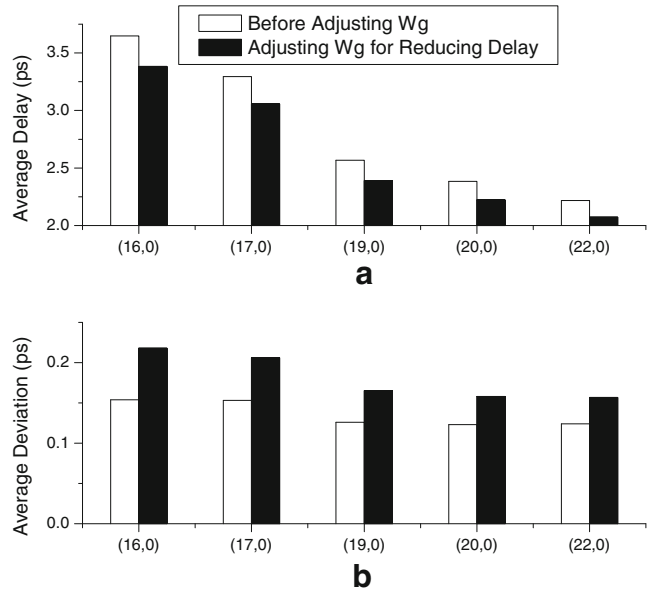


Fig. 18 Delay and deviation vs. N_{CD} when adjusting W_g for reducing delay (Algorithm 2) at different chiralities (V_{GS}=0.9 V, (19,0), N=9, W_g=32 nm)

$$\begin{aligned} W_g' &= W_g - W_{Rg} \\ &= W_g - s' - d \\ &= W_g - \left(s - 2 \times \frac{d}{2}\right) - d \\ &= W_g - s \end{aligned} \tag{7}$$

The proposed method for adjusting W_g is depicted in Fig. 15. In Fig. 15a, there is an undeposited CNT at the leftmost position, so W_g is reduced until a deposited CNT is found (at a new width W_g'); so in this step, P_{CD} is also changed to P_{CD}'. An 'X' in P_{CD} means that the (deposited or undeposited) CNT is not included in

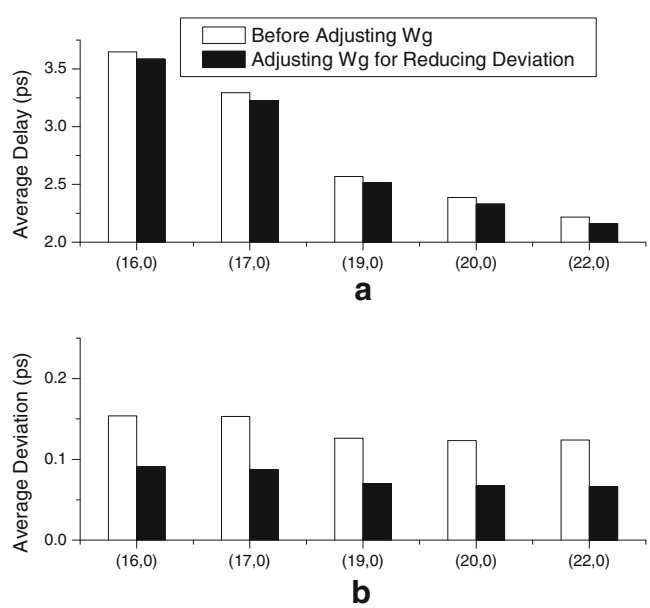


Fig. 19 Delay vs. N_{CD} when adjusting W_g for reducing deviation (Algorithm 3) at different chirality values (V_{GS}=0.9 V, (19,0), N=9, W_g=32 nm)

the adjusted gate width. When a deposited CNT is found on the leftmost position, the proposed method checks whether there is at least a undeposited CNT to the right of the deposited CNT. If undeposited CNT(s) exist(s), the deposited CNT(s) is (are) discarded (denoted by P_{CD}'') and the delay for P_{CD}' and P_{CD}'' are compared (Fig. 15b). If the delay for P_{CD}'' is smaller than for P_{CD}', W_g' is reduced to W_g'' (Fig. 15c). These steps for the discarding process are repeated until the delay cannot be decreased any longer. Figure 15d shows the process when the same method is applied from right to left (W_g'' is reduced to W_g''). When N_{CD} is known, various P_{CD}s can then exist (N_{CCD}) (as found previously in Eq. 1). The proposed method for adjusting W_g is applied to these P_{CD}s. This algorithm is referred to as Algorithm 2.

By applying Algorithm 2, the delay can be reduced (Fig. 16); the plots with white symbols in Fig. 16 represent the delay values from Fig. 4 and the plots with black symbols represent the delay values as reduced by using Algorithm 2. The largest delay cannot be decreased when N_{CD} is 4, because all CNTs are deposited with the same interval and two CNTs are at the edge of the CNTFET; so, a CNT must be undeposited to reduce the gate width. Moreover, the delay cannot be decreased due to the small distance between CNTs. The delay is reduced on average by 6.981 %, 1.183 %, and 8.925 % for the average, largest, and the least delay values respectively (at a CNT chirality of (19,0)).

7 Adjustment for Reduced Delay Deviation

In Fig. 4, when the probability of undeposited CNTs during CNTFET manufacturing is less than 20 %, the deviation is less than 7 %; however, if the probability of undeposited CNTs is larger than 20 %, the deviation substantially increases as N_{CD} increases [3]. As discussed previously, Algorithm 2 reduces the delay but the delay deviation may increase after adjusting W_g. To overcome this drawback prior to adjusting the gate width, the reduced delay ($Delay_{Rgg,CNTFET}$) is compared with $Delay_{least}$ (Fig. 4) and $Delay_{gg,CNTFET}(i)$ (lines 15 and 35 in Algorithm 2, respectively) . The delay is reduced only when $Delay_{Rgg,CNTFET}$ is larger than $Delay_{least}$ and less than $Delay_{gg,CNTFET}(i)$. So an additional 'for loop' is required to determine the least delay as dependent on N_{CD}.

This method is therefore a modification to Algorithm 2; the algorithm for W_g adjustment for reducing the deviation is hereafter referred to as Algorithm 3. The simulation results of Algorithm 3 are depicted in Fig. 17. Compared to the results plotted in Fig. 4, Algorithm 3 reduces the deviation by 44.444 % with a 2.141 % delay reduction. When the original Algorithm 2 is applied to Fig. 4, the delay is reduced by 6.968 % but the deviation is increased by 30.952 % (Fig. 16). Therefore, an improvement of 75.397 % in deviation is achieved at the expense of a 4.827 % delay degradation by utilizing Algorithm 3. These percentage values are depicted in Fig. 20 (chirality is (19,0)). Even though a different algorithm (Algorithm 3) is utilized, when N_{CD} is 4 (Fig. 17), the largest delay cannot be decreased as also applicable to Algorithm 2 and explained previously.

```
01 Algorithm  Adjusting W_g for P_CD
02 begin
03   for i to N_CCD
04     if 0 exists on the leftmost position in P_CD(i)
05       W_g is reduced until 1 is found and stored in W_Rg(i)
06          Delay_gg,CNTFET(i)=Delay(P_CD(i), W_Rg(i))
07       end
08       stop=0
09       while (stop=0)
10         if 0 exists on the right of leftmost 1
11             Delay_gg,CNTFET(i)= Delay(P_CD(i), W_g(i))
12             the leftmost 1 is changed to 0 and stored in P_RCD
13             W_g is reduced until 1 is found and stored in W_Rg
14             Delay_Rgg,CNTFET=Delay(P_RCD, W_Rg)
15             if Delay_Rgg,CNTFET < Delay_gg,CNTFET(i)
16                 Delay_gg,CNTFET(i)= Delay_Rgg,CNTFET
17             else
18                 stop=1
19           end
20         end
21       end
22   end
23   for i to N_CCD
24       if 0 exists on the rightmost position in P_CD(i)
25         W_g is reduced until 1 is found and stored in W_Rg(i)
26         Delay_gg,CNTFET(i)=Delay(P_CD(i), W_Rg(i))
27       end
28       stop=0
29       while (stop=0)
30         if 0 exists on the left of rightmost 1
31             Delay_gg,CNTFET(i)= Delay(P_CD(i), W_g(i))
32             the rightmost 1 is changed to 0 and stored in P_RCD
33             W_g is reduced until 1 is found and stored in W_Rg
34             Delay_Rgg,CNTFET=Delay(P_RCD, W_Rg)
35             if Delay_Rgg,CNTFET < Delay_gg,CNTFET(i)
36                 Delay_gg,CNTFET(i)= Delay_Rgg,CNTFET
37             else
38                 stop=1
39             end
40           end
41         end
42     end
43 end
```

Algorithm 2. Algorithm for W_g adjustment

Algorithms 2 and 3 have also been applied to CNTFETs with different chirality vectors. As shown in Fig. 18 and 19, nearly the same performance with respect to reducing the delay and its deviation is achieved regardless of the change in chirality. Figure 20 shows the reduction in average delay and deviation by considering the chirality vectors, when Algorithm 2 and Algorithm 3 are applied (the increase has a negative value in Fig. 20). When Algorithm 2 is applied, the delay is decreased on average by 6.968 % while the average deviation increases by 32.444 % on average. However, when Algorithm 3 is applied, the average deviation is decreased by 44.195 % on average, while the average delay

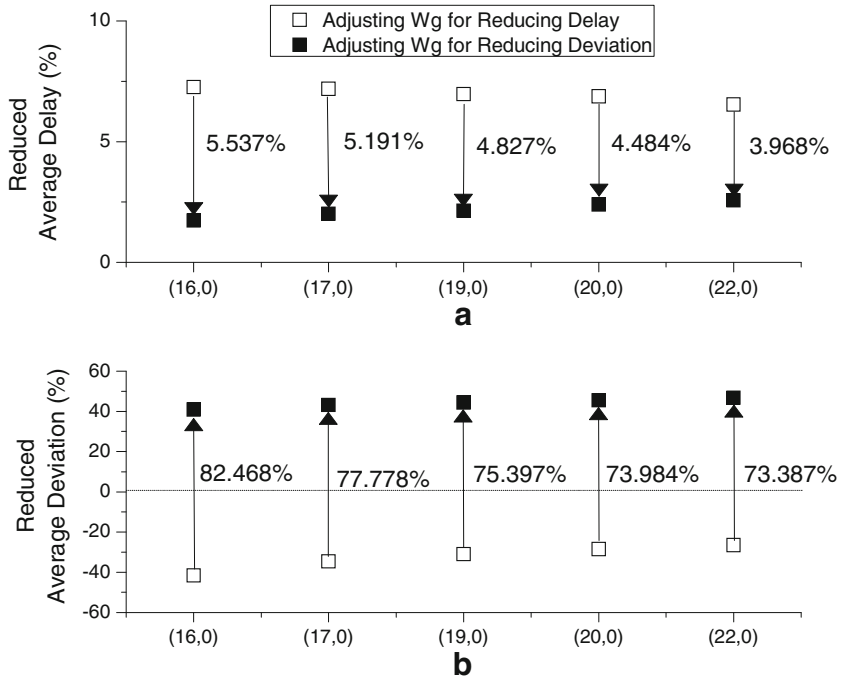


Fig. 20 Reduction in average delay (%) and average deviation between average delay and least delay (%) vs. chirality when adjusting W_g for reducing delay (Algorithm 2) and deviation (Algorithm 3) (V_{GS}=0.9 V, N=9, W_g=32 nm)

reduction is 2.166 % on average. So, Algorithm 3 achieves a 76.603 % on average improvement at the expense of a 4.801 % on average degradation in delay.

Figures 21 and 22 show both the reduction in average delay and deviation when the two proposed methods are probabilistically applied to the delay values of Fig. 10 at various chirality and standard deviation values (the increased value has a negative value in Figs. 21 and 22). Figure 21 shows that the reduced average delay values by using Algorithm 2 are larger than those by using Algorithm 3 because, as mentioned above, Algorithm 2 reduces the delay as much as possible at the expense of an increase of the deviation. When the standard deviation increases, the reduction in average delay increases with both Algorithms 2 and 3 (Fig. 21) because in this case, larger delay values can be encountered (Fig. 10) and the proposed algorithms reduce the larger delay values (so, average delay values are eventually reduced).

Otherwise, when the standard deviation is increased, Algorithm 3 can reduce deviation (black triangular symbols have bigger values than black triangular symbols) as shown in Fig. 22 because the purpose of Algorithm 3 is reducing deviation. However, the effect of Algorithm 3 is reduced as chirality is increased because, as shown in Fig. 13, the deviation is decreased as chirality is increased. When deviation is

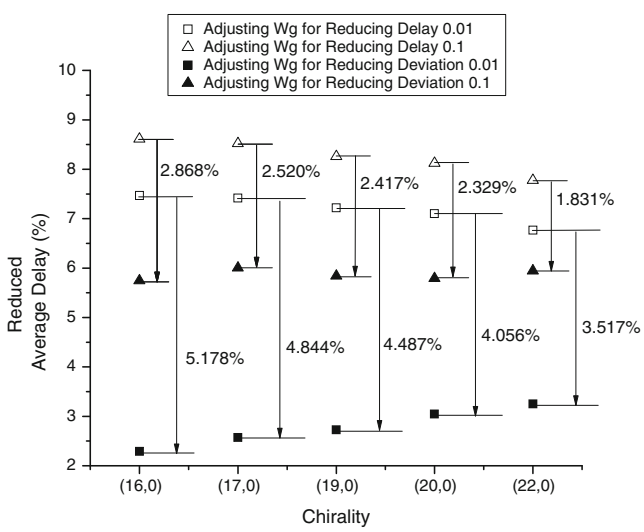


Fig. 21 Reduction in average delay (%) vs. yhirality when adjusting W_g for reducing delay (Algorithm 2) and deviation (Algorithm 3) at standard deviation values of 0.01 and 0.1 (V_{GS}=0.9 V, N=9, W_g=32 nm)

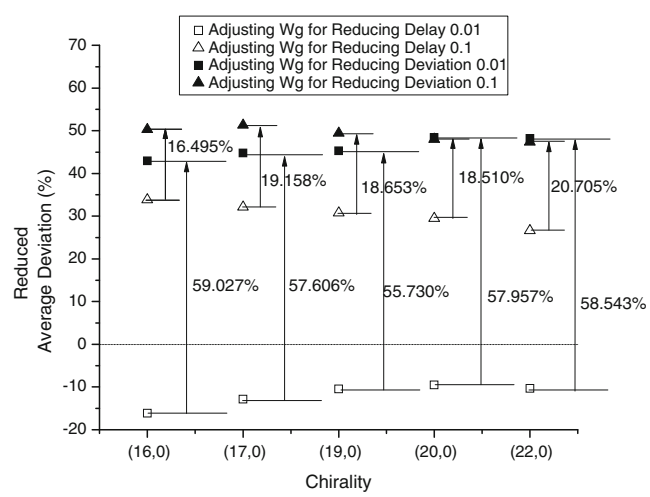


Fig. 22 Reducion in average deviation (%) vs. chirality when adjusting W_g for reducing delay (Algorithm 2) and deviation (Algorithm 3) at standard deviation values of 0.01 and 0.1 (V_{GS}=0.9 V, N=9, W_g=32 nm)

Table 2 Summary of results of proposed methods by adjusting W_G

Analysis method			Reduction in average delay (%)		Reduction in average deviation (%)		Difference (%)	
	Chirality	σ	adjusting W_g for reducing delay	adjusting W_g for reducing deviation	adjusting W_g for reducing delay	adjusting W_g for reducing deviation	adjusting W_g for reducing delay	adjusting W_g for reducing deviation
DA	(16,0)	N/A	7.264	1.727	−41.558	40.909	5.537	82.468
	(17,0)		7.195	2.004	−34.641	43.137	5.191	77.778
	(19,0)		6.968	2.141	−30.952	44.444	4.827	75.397
	(20,0)		6.873	2.389	−28.455	45.528	4.484	73.984
	(22,0)		6.537	2.570	−26.613	46.774	3.968	73.387
PA	(16,0)	0.01	7.468	2.291	−16.102	42.925	5.178	59.027
		0.05	8.326	4.277	10.684	47.617	4.048	36.933
		0.1	8.615	5.746	33.842	50.337	2.868	16.495
	(17,0)	0.01	7.418	2.574	−12.830	44.776	4.844	57.606
		0.05	8.236	4.521	10.876	48.036	3.715	37.159
		0.1	8.523	6.003	32.180	51.338	2.520	19.158
	(19,0)	0.01	7.216	2.729	−10.420	45.310	4.487	55.730
		0.05	7.978	4.622	11.103	47.630	3.356	36.527
		0.1	8.260	5.843	30.768	49.421	2.417	18.653
	(20,0)	0.01	7.101	3.045	−9.541	48.416	4.056	57.957
		0.05	7.846	4.692	10.972	46.866	3.153	35.893
		0.1	8.122	5.793	29.498	48.008	2.329	18.510
	(22,0)	0.01	6.769	3.252	−10.328	48.215	3.517	58.543
		0.05	7.518	4.808	9.452	45.882	2.710	36.431
		0.1	7.777	5.946	26.660	47.365	1.831	20.705

small (deviation is 0.01), Algorithm 2 increase deviation as mentioned before; so, white triangular values have minus values in Fig. 22. However, when the standard deviation is increased from 0.01 to 0.1, Algorithm 2 can also decrease the deviation, because a larger delay can be encountered (Fig. 10) at higher values of standard deviation; so, the deviation can be decreased by reducing the the larger and average values with Algorithm 2.

The summary of the results for the two proposed methods (Algorithm 2 and Algorithm 3) under DA and PA is provided in Table 2. Table 2 shows that the simulation results between DA and PA are similar.

- In DA Algorithm 2 reduces the delay by 6.968 %, but the deviation is increased by 32.444 %. Algorithm 3 reduces the deviation by 44.159 % with a 2.166 % delay reduction.
- In PA, Algorithm 2 reduces the delay and deviation by 7.811 % and 9.788 % respectively. Algorithm 3 reduces the deviation by 47.476 % with a 4.409 % delay reduction.

8 Conclusion

This paper has presented a detailed analysis (inclusive of related algorithms) and extensive simulation results to estimate the effect of undeposited CNTs in a CNTFET. The analysis considers the number and position of the undeposited CNTs using the model of [3]. The presented analysis has shown that the delay drastically increases as the number of undeposited CNTs is increased and a significant deviation is present as related to the position of the undeposited CNTs. When the undeposited CNTs are grouped together (the deposited CNTs are separated by small intervals), the delay has the least value. However, when the deposited CNTs are separated by the largest intervals, then the delay is also the largest. A probabilistic analysis also has been presented to estimate the impact of the number and position of the undeposited CNTs.

Next, based on the capabilities of current lithographic technology, two methods for adjusting the gate width have been proposed; these methods adjust and remove CNTs at the gate. Using these methods, the delay and deviation can be reduced. Using the first method for adjusting the gate width, the average delay can be decreased by 6.968 %. However, the deviation is increased by 32.444 %. To decrease this deviation, a second method has been proposed; this method decreases the gate width only when the decreased value is above the least delay. To verify these two approaches, a probabilistic analysis has also been performed by utilizing normal and uniform distributions. The analysis has shown that the simulation results from the deterministic analysis and

the simulation results based on a probabilistic analysis are almost similar. In the deterministic analysis, the first gate adjustment method shows that the average delay can be reduced by 7.014 %, but the deviation is increased by 32.941 %. The second gate adjustment method reduces the deviation by 43.971 % with 2.111 % delay reduction. In the probabilistic analysis, the first method reduces the delay and the deviation by 7.811 % and 9.788 % respectively. The second method reduces the deviation by 47.476 % with 4.409 % delay reduction.

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